

**REMARKS**

Claims 1-3, 5, 7-8, 11-12, 14, 19, 20, 24, 30 and 32-34 are pending. By this Amendment, claims 1, 5, 7, 11, 14, 19, 24, and 32-34 are amended; claims 4, 6, 9, 10, 13, 15-18, 21-23, 25-29 and 31 are cancelled.

The Office Action sets forth an objection to the disclosure based on noted informalities. Applicant's present amendments to the specification address the noted informalities in accordance with the Examiner's suggestions.

Claims 1-34 were rejected under 35 U.S.C. §112, second paragraph, for alleged indefiniteness. Applicant's amendments to the claims provide clarifications responsive to the issues raised in the Office Action. Reconsideration and withdrawal of the rejections are respectfully requested in view of applicant's clarifying amendments.

Claims 1-34 were rejected under 35 U.S.C. §102(b) as allegedly being anticipated by Quayle et al. U.S. Patent No. 6,694,464. It is respectfully submitted that Quayle et al. fails to teach or suggest the inventions of the amended claims.

As amended, the clarified subject matter of dependent claims 4 and 6 is incorporated into independent claim 1. This subject matter specifies that at least one of the emulation ICs "comprises on-chip data processing resources to cooperate and assist said onboard data processing resources to perform said local generation and application of testing stimuli."

Similarly, claim 7 is amended to incorporate clarified subject matter of dependent claims 9 and 10, which subject matter specifies that "at least some of said generation of testing stimuli are performed by on-chip data processing resources of said emulation ICs."

Similarly, independent claim 11 is amended to incorporate the subject matter of dependent claim 13, which specifies that "at least one of said emulation ICs comprises on-chip

data processing resources to cooperate with and assist said on-board data processing resources to perform said local generation and application of testing stimuli.”

Similarly, independent claim 14 is amended to incorporate the subject matter of dependent claim 15, specifying that “at least some of said generation of testing stimuli are performed by on-chip data processing resources of said emulation ICs.”

Similarly, independent claim 19 is amended to incorporate the subject matter of dependent claim 21, which specifies that “at least one of said emulation ICs of said logic boards comprises on-chip data processing resources to cooperate with and assist the on-board data processing resources of the logic board to perform said local and corresponding generation and application of testing stimuli.”

Similarly, independent claim 24 is amended to incorporate the subject matter of dependent claim 25, which specifies that “at least some of said performances of local and corresponding generation and application of testing stimuli are assisted by on-chip data processing resources of the emulation ICs of the logic boards.”

Independent claim 30 is amended to incorporate clarified subject matter of claim 31, specifying that the recited method further comprises “locally generating testing stimuli using said on-chip data processing resources; and locally applying the generated testing stimuli to an IC design being emulated, using said on-chip data processing resources.”

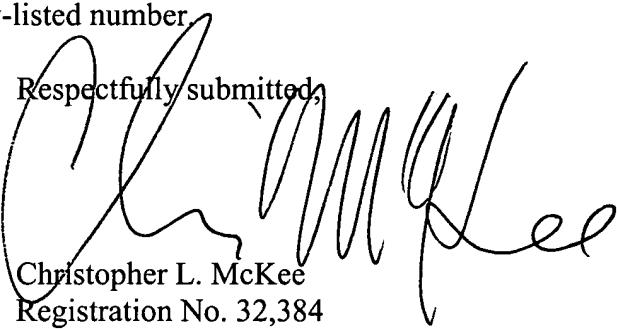
Similarly, clarified independent claim 32, directed to an “emulation integrated circuit (IC),” specifies that “on-chip data processing resources ... locally generate testing stimuli, and locally apply the generated testing stimuli to at least one of said emulation circuit elements.”

Clarified independent claim 34 recites steps of “locally generating on said emulation IC testing stimuli, using on-chip data processing resources, and locally applying the testing stimuli, using said on-chip data processing resources, to at least one of said emulation circuit elements.”

Contrary to the Office Action, Quayle et al. do not teach on-chip data processing resources used to generate and/or apply emulation IC testing stimuli. Regarding this feature, the Office Action cites Quayle et al. Figure 20c, and event signal output 236. See, e.g., Office Action p. 10, paragraph 6. However, events signal outputs 236 are not testing stimuli. Rather, as described at column 23, lines 63-66 of Quayle et al., event signal outputs 236 are combinations of signal states in the design undergoing emulation which are generated inside the logic chips 10 and 204 on the logic boards 200. Thus, the Quayle et al. patent does not anticipate any of independent claims 1, 7, 13, 14, 19, 24 30, 32 and 34 (or the claims depending therefrom).

In connection with claim 32, the Office Action also refers (at pp. 19-20, Section 7.11) to clock generation chip 204 (Fig. 19) for the feature of locally generating testing stimuli and locally applying the generated testing stimuli. However, chip 204 is not an emulation integrated circuit (IC). Nor do Quayle et al. teach that CoSim logic chip 204 generates or applies testing stimuli (note that column 22, lines 54-55 explains that clock generation logic chip 204 is the CoSim logic chip). Rather, Quayle et al. describe that “[d]esign signals may be sampled in the logic chips 10 and CoSim logic chip 204,” that these chips are “attached to an event bus 212 and a clock in bus 214,” and that “the event bus is used to route event signals from within the logic chips 10 and CoSim logic chip 204 to logic analyzer control circuitry.” See the paragraph bridging columns 17 and 18, and the immediately following paragraph in column 18.

For all of the foregoing reasons, it is respectfully submitted that this application is in condition for allowance. Should the Examiner believe that anything further is desirable in order to place the application in even better form for allowance, he is respectfully urged to telephone applicant's undersigned representative at the below-listed number.

Respectfully submitted,  
  
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